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A novel voltage reference without the operational amplifier and resistors

Jin Ling Zhou, WanLing Deng, XiaoYu Ma, JunKai Huang
(College of Information Science and Technology, Jinan University, China)

ABSTRACT*: A novel voltage reference has been proposed and simulated using a 0.18μm CMOS process in this paper. A near-zero temperature coefficient voltage is achieved in virtue of the bias voltage subcirciut which consists of two MOSFETs operating in the saturation region. The kind of bias voltage subcirciut is used to adjust the output voltage and compensate the curvature. The output voltage is equal to the extrapolated threshold voltage of a MOSFET at absolute zero temperature, which was about 591.5 mV for the MOSFETs we used. The power supply rejection ratio (PSRR) is improved with three feedback loops. Although the output voltage fluctuates with process variation, the circuit can monitor the process variation in MOSFET threshold voltage. The simulation results show that the line regulation is 0.75 mV/V in a supply voltage range from 1.6 V to 3.1 V and the temperature coefficient is around 10.8 ppm/℃ to 28.5 ppm/℃ at 9 different corners in a temperature range from -20℃ to 120℃. The PSRR is -70 dB at 100Hz with a supply voltage at 1.8 V, and the layout size is 0.012mm^2. The results of simulation and post layout simulation are almost the same.*
Keywords*: CMOS, voltage reference, PSRR, saturation region, process variation*

I. Introduction

The voltage references are essential modules in integrated circuit designs, which are used in analog -to-digital or digital-to- analog conversion, current sources for driving laser diodes, signal conditioning, signal measurement, power supply, battery charges, and battery supervision, etc. However, different circuit topologies operated at different frequencies induce significant fluctuations on the power supply. Therefore, a larger PSRR is required. Some circuits enhance the PSRR with operational amplifier [1-3]. However, the operational amplifier brings Offset Voltage and increases the complexity of the circuit. In order to avoid the Offset Voltage brought from the operational amplifier, several feedback loops are designed in the circuit. The traditional voltage reference circuit needs resistance of several hundred mega ohms to adjust circuit for temperature compensation [4-6]. Such a high resistance needs large area. Therefore, in order to avoid the use of resistance which results in a large chip area, and to eliminate the process variations caused by the resistance manufacturing, we develop a new voltage reference without resistors.

In this paper, a novel voltage reference is presented. It uses the feedback technique instead of operational amplifier to enhance PSRR. The PSRR is analyzed in a small signal model and simulation results show that it has been improved greatly. The temperature compensation is obtained using the bias voltage subcirciut which consists of two MOSFETs operating in the saturation region and is used to adjust the output voltage and compensate the curvature. The output voltage is equal to the threshold voltage when the MOSFET operates at 0 K. In this paper, the output voltage is about 591.5 mV. The results of process corner simulation show that the output voltage variation ΔVref well reflects the threshold voltage variation ΔV_{TH} and temperature coefficient (TC) of output voltage hardly depends on process variation. Post layout simulation shows the parasitic parameters of this circuit are very small. The following sections provide the details on our circuit. Section 2 describes the principle of our voltage reference source. Section 3 presents the simulation results. Section 4 presents the layout and post layout simulation results and comparison. Finally, Section 5 shows the conclusion.

II. Circuit and principle

The principle of our voltage reference is illustrated in Fig.1. The circuit consists of a start-up circuit, a current source subcircuit and a bias voltage subcirciut. The bias voltage subcirciut consists of two MOSFETs (MN6, MP4). All the MOSFETs except for MN4 operate in the saturation region. The MOS resistor MN4 operates in the strong-inversion and deep-triode region. The circuit generates two voltages with a negative temperature coefficient (TC) and a positive TC. Then, it adds them together to produce a constant voltage with a zero TC. The following sections describe the operation in detail.

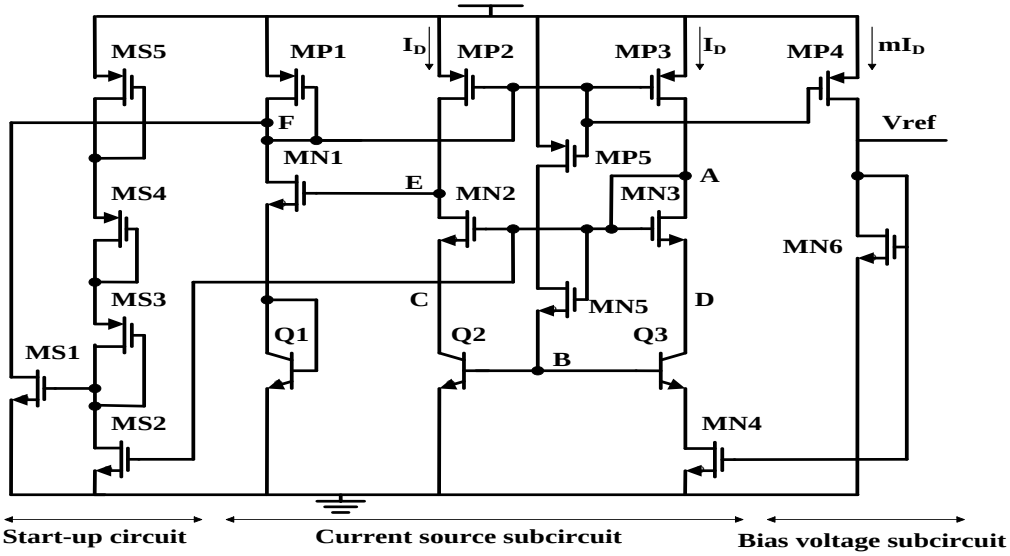

Fig.1The proposed voltage reference circuit

2.1 Principle of temperature compensation

In the saturation region, the gate-source voltage is given by [7]:

$$V_{GS} = V_{TH} + \sqrt{2I_D / (\mu C_{OX} K)} \tag{1}$$

Where K is the aspect ratio (=W/L) of the transistor, μis the carrier mobility, C_{OX} is the gate-oxide capacitance per unit area, and V_{TH} is the threshold voltage of MOSFET.

In the current source subcircuit, the base-emitter voltage V_{BE2} in Q_2 is equal to the sum of the base-emitter voltage V_{BE3} inQ_3 and the drain-source voltage V_{DSM4} inMN_4:

$$V_{BE2} = V_{BE3} + V_{DSM4} \tag{2}$$

The base-emitter voltage $V_{BE}=V_T\ln(I_C/I_S)$, where V_T is the thermal voltage, $I_S$is the scale current which is proportional to the base-emitter area and I_C is the collector current of the bipolar transistor [8]. Combining with (2), V_{DSM4} can be written as $V_{DSM4}=V_T\ln(N)$, where N is the area ratio of emitters inQ3 and Q2. MOS resistorMN4 operates in the strong-inversion, deep-triode region.Its resistance R_{M4} is given by[1]:

$$R_{M4} = \frac{1}{K_{M4}\mu C_{OX}(V_{GS4} - V_{TH})} \tag{3}$$

Therefore,the following expression is obtained as:

$$I_D = \frac{V_{DSM4}}{R_{M4}} = K_{M4}\mu C_{OX}(V_{GS4} - V_{TH})V_T \ln(N) \tag{4}$$

The threshold voltage is expressed as $V_{TH}=V_{TH0}$-kT, where V_{TH0} is the threshold voltage at 0Kand k is the TC of V_{TH} [1]. Given $I_{D6}=mI_D$ and using the relation of $Vref=V_{GS4}=V_{GS6}$ from the circuit, we find that the output voltageVref of the circuit can bederived as:

$$Vref = V_{TH} + \sqrt{2I_{D6} / (\mu C_{OX} K_6)} = V_{TH0} - kT + \sqrt{\frac{2mK_{M4}(V_{GS4} - V_{TH0} + kT)V_T \ln(N)}{K_6}} \tag{5}$$

where $V_T=k_BT/q$, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge. In regulate circuit, when TC has the smallest value,the relation of$Vref=V_{GS4}=V_{GS6}=V_{TH0}$ can bedeveloped. As a result, Vrefis rewritten as:

$$Vref = V_{TH0} + T\left\{\sqrt{\frac{2mK_{M4}kk_B \ln(N)}{qK_6}} - k\right\} \tag{6}$$

By (6), we find that a zero TC can be achieved with the condition of:

$$\frac{2mK_{M4}k_B \ln(N)}{qK_6} = k \tag{7}$$

According to (7), a zero TC voltage can be obtained by choosinga proper W/L.Moreover, from (6), we have:

$$Vref = V_{THO} \tag{8}$$

2.2 Principle of enhanced PSRR

As shown in Fig.1,the circuit shows a high insensibility to the supply variations. PSRR is enhanced by three feedback loops. In this circuit, the negative feedback is much greater than the positive feedback and our aim is to improve PSRR with negative feedback. Therefore, we ignore thepositive feedback in following analysis. There are three negative feedback loops in this design, i.e., negative feedback loop A-E-F-A， A-B-C-E-F-A and A-B-D-A. Ignoring channel length modulation effect and body effect, ΔI_D can be written as:

$(\Delta V_{DD} - \Delta V_F) g_{mP3} = \Delta I_D$ （9）

The expression of feedback coefficient *a* from A to F can be expressed as:

$$a = \frac{\Delta V_F}{\Delta V_A} \tag{10}$$

where*a* is caused by feedback A-E-F and A-B-C-E-F. Therefore, we get the following expression:

$$\frac{\Delta V_F}{\Delta V_A} = \frac{\Delta V_F}{\Delta V_E}\frac{\Delta V_E}{\Delta V_A} + \frac{\Delta V_F}{\Delta V_E}\frac{\Delta V_E}{\Delta V_C}\frac{\Delta V_C}{\Delta V_B}\frac{\Delta V_B}{\Delta V_A} \tag{11}$$

where:

$$\frac{\Delta V_F}{\Delta V_E} \approx -\frac{g_{mN1}}{1+g_{mN1}r_{Q12}}[\frac{1}{g_{mP1}} // (1+g_{mN1}r_{oN1})r_{Q12}] \tag{12}$$

$$\frac{\Delta V_E}{\Delta V_A} \approx -\frac{g_{mN2}}{1+g_{mN2}r_{Q12}}[r_{oP2} // (1+g_{mN2}r_{oN2})r_{Q12}] \tag{13}$$

$$\frac{\Delta V_B}{\Delta V_A} \approx \frac{g_{mN5}r_{BG}}{1+g_{mN5}r_{BG}} = 1 \tag{14}$$

$$\frac{\Delta V_C}{\Delta V_B} \approx -\frac{\beta r_{CV}}{r_{be}} \tag{15}$$

$$\frac{\Delta V_E}{\Delta V_C} \approx g_{mN2}[r_{oP2} // (1+g_{mN2}r_{oN2})r_{Q12}] \tag{16}$$

Combining (4)~(8) and (3), *a* can be rewritten:

$$a = \frac{\Delta V_F}{\Delta V_A} \approx \frac{r_{oP2}}{r_{Q12}^{\ 2} g_{mP1}} + \frac{r_{oP2}g_{mN2}\beta r_{CV}}{r_{Q12}g_{mP1}r_{be}} >> 1 \tag{17}$$

where$\Delta V_A = \Delta I_D r_{oA}$, and $r_{oA}$is the output impedance at point A. Combining (9) and (10), we obtain:

$$\frac{\Delta I_D}{\Delta V_{DD}} = \frac{g_{mP3}}{1+ar_{oA}g_{mP3}} \tag{18}$$

The loop gain A_{loop} of feedback loop A-B-D-A can be written as

$$A_{loop} \approx -\frac{\beta r_{DV}}{r_{be}+(1+\beta)R_{M4}} < 0 \tag{19}$$

When assuming ΔV_A is the voltage change at point A, due tothe role of the feedback loop A-B-D-A, the feedback voltage becomes $\Delta V_A A_{loop}$ at point A. Therefore, considering the feedback loop, the total voltage change is $\Delta V_A + \Delta V_A A_{loop}$ at point A. Since we have$(\Delta V_A + \Delta V_A A_{loop})/\Delta V_A = (1+A_{loop})$ and consider the loop gain A_{loop}, the PSRR of current I_D can be expressed as:

$$PSRR_{I_D} = \frac{\Delta I_D}{\Delta V_{DD}} = \frac{g_{mP3}(1+A_{loop})}{1+ar_{oA}g_{mP3}} \tag{20}$$

For regulate circuit, the relation $-1<A_{loop}$is valid. Combining with (12),we obtain $-1<A_{loop}<0$. Using (5) and $I_{D6}=mI_D$, we get the PSRR of output voltage as:

$$\text{PSRR} = \frac{\Delta Vref}{\Delta V_{DD}} = \sqrt{\frac{2mPSRR_{I_D}}{\Delta V_{DD}\mu C_{OX}K_6}} \tag{21}$$

In (9)~(21), ΔV_{DD} refers to the amount of change of supply voltage V_{DD}, g_m and r_o are defined as the transconductance and output resistance of the transistors, respectively, subscript "N" means N-type, subscript "P" means P-type, and subscript number means the number of the transistors. Parameter r_{Q12} is the output

resistance of Q1,Q2, r_{DV} and r_{CV} is the resistance seen from D or C to V_{DD}, r_{BG} is the resistance seen from B to ground, β is current gain of Q1 and Q2, and r_{be} is the resistance between the base and emitter of bipolar transistor.

In the circuit, since ^{a} >>1 and -1<A_{loop}<0, the value of PSRR of output voltage is very small.Consequently, the PSRR is enhanced greatly by these three negative feedback loops.

The negative feedback loop A-B-C-E-F-A and A-B-D-A are associated with MN5. So we design the aspect ratio (=W/L) of MN5 in order to have a better PSRR and it do not change fast when supply voltage varies.

2.3 Process variation

According to (6), TC of Vref can be expressed as:

$$TC = \frac{\mathrm{dVref}}{\mathrm{dT}} = \sqrt{\frac{2mK_{M4}kk_B \ln(N)}{qK_6}} - k \tag{22}$$

In this expression, parameters m, k_B, N and q are constant and independent of the process variation. Due tothe process variations, the effect on the relative accuracy of the parameters K_{M4} and K_6 can be reduced by using large-sized transistors.In addition, k shows a very small dependency on process variation [1]. Therefore, the TC of the output voltage becomes much lessdependent on process variation. V_{TH} isgiven by [1]:

$$\mathrm{V_{TH}} = -\frac{E_g}{2q} + V_T \ln(\frac{N_A}{n_i}) + \frac{\sqrt{4\varepsilon_{si}qN_AV_T \ln(N_A / n_i)}}{C_{OX}} \tag{23}$$

whereε_{si} is the silicon permittivity, $N_A$is the channel doping concentration, $n_i$is the intrinsic carrier density, and E_g is the bandgap energy of silicon. Since V_{TH} is a function of N_A and V_{TH}=V_{TH0}-kT, V_{TH0} varies with the change of N_A. Here,ΔV_{TH},ΔV_{TH0},ΔVref mean the variation of V_{TH}, V_{TH0},Vrefdue to theprocessvariation.As a result,$\Delta V_{TH} \approx \Delta V_{TH0}$=$\Delta$Vrefcan be obtained.

III. Simulation results

The proposed circuit is verifiedby simulationwith a 0.18μm CMOS technology. Fig.2 shows the simulation results of the temperature dependency of the voltagereference in the range from -20℃ to 120℃, where the supply voltage varies from 1.8 V to 3.0 V. The simulation TC is around 10.8 ppm/℃ with a supply voltage at 1.8 V and the output voltage is about 591.5 mV. Fig.3 shows the PSRR at room temperature without any filtering capacitor, where the supply voltage alsovaries from 1.8 V to 3.0 V. The highest PSRR is -70 dB at 100 Hz with the supply voltage of 1.8 V. The lowest PSRR is -53 dB at 100 kHz at the supply voltage of 3.0 V. Although PSRR changes with different supply voltages, it is always less than -53 dB, which clearly shows that these three feedback loops is useful. Fig.4 shows the output voltage as a function of supply voltage at room temperature. The circuit operates correctly when the supply voltage is higher than 1.6 V. The line regulation is 0.75 mV/V when the supply voltage ranges from 1.6 V to 3.1 V. Thus, the proposed scheme is able to achieve the voltage reference that is almost independent of temperature and supply voltage. The temperature dependence of Vref and V_{TH} are shown in the Fig.5. CurvesVrefmos_ttbjt_tt, Vrefmos_ffbjt_tt, and Vrefmos_ssbjt_tt are similar and parallel with each other.Analogously,curves V_{TH}mos_ttbjt_tt, and V_{TH}mos_ffbjt_tt,V_{TH} mos_ssbjt_ttbehave in the same way. In addition, we have ΔVref/$\Delta V_{TH} \approx 1$ in thetemperature of 25℃.Therefore, the outputvoltagevariation ΔVref reflectsthe threshold voltagevariation ΔV_{TH}.Although the output voltage depends on process variation, by utilizing $\Delta\mathrm{Vref} \approx \Delta V_{TH}$, the circuit can monitor the process variation in MOSFET threshold voltage and provides a process compensation for the corresponding systems. As a result, this design has its practical value. Fig.6 shows PSRR at different process corners at 1.8 V. The highest PSRR is -74.6 dB at 100 Hz when corner of MOS is SS and corner of BJT is TT. The lowest PSRR is -68.1 dB at 100 Hz when corner of MOS is FF and corner of BJT is TT. Therefore PSRR is insensitive to process variation.Fig.7 shows the temperature characteristics of the output voltage for 9 corners, corresponding to the permutation of Fast, Slow and Typical corners of NMOS, PMOS and BJT transistors. The maximum deviation of output voltage at different process corners is more than 60mv. Howeverin fact, the variation of the reference voltage becomes smaller than process corners simulation [1], because the chips are fabricated from the same water. TC from 10.8 ppm/℃ to 28.5 ppm/℃were simulated at 9 different corners. This shows that the TC of the output voltage has a smaller dependence on process variation.

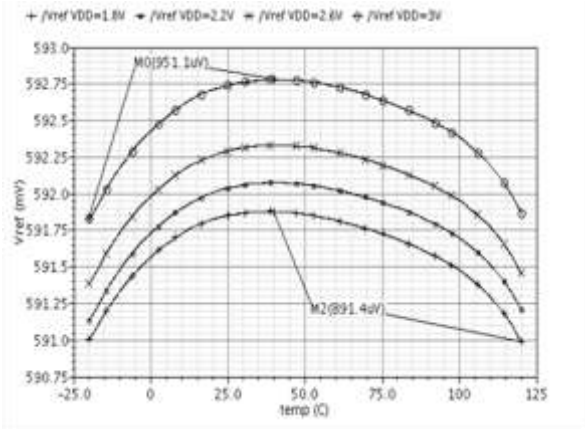

Fig.2Output voltage Vref versus temperature with

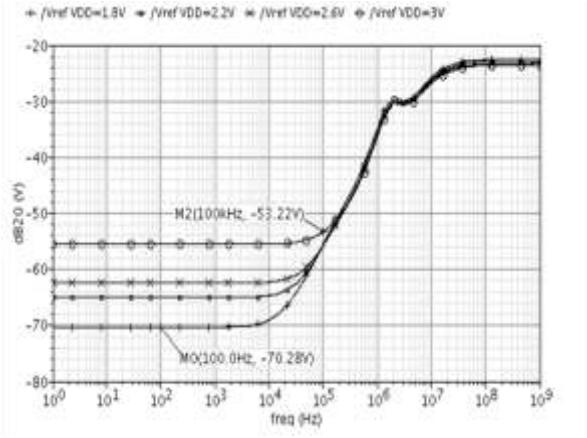

Fig.3PSRR versus frequency at different supply various supply voltages voltages

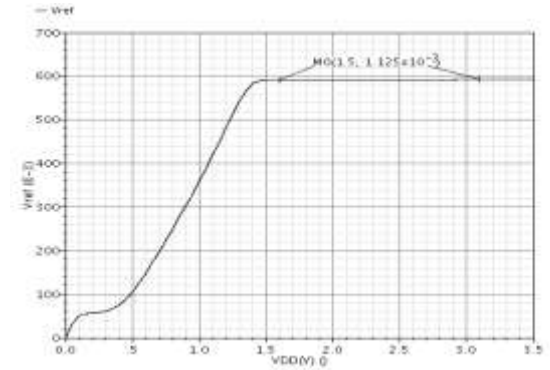

Fig.4Vref versus supply voltage at room temperature

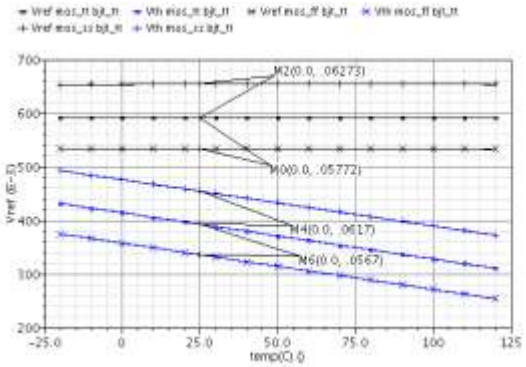

Fig.5Vref/V_{TH} versus temperature for different process corners at 1.8 V

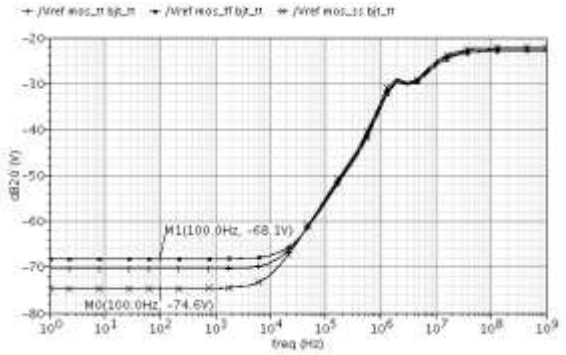

Fig.6PSRR versus frequency at different process

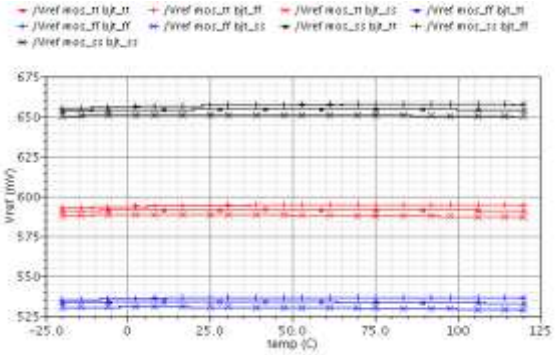

Fig.7Output voltage Vref versus temperature with corners at 1.8 Vvarious process corners at 1.8 V

IV. Layout and post layout simulation

Fig.8 displays the layout of the proposed design, and the layout size is 0.012mm2 (100um*120um). The comparison of output voltage Vref as a function of temperature between simulation and post layout simulation is shown in Fig.9. Curve with plus signs is the simulation curve and the other one is the post layout simulation curve. They are very similar and the maximum deviation is 39.92uv. Fig.10 shows the comparison of PSRR versus frequency. The curves of simulation and post layout simulation almost overlap when frequency is less than 10KHz. These two simulation results are almost the same, which shows that the parasitic parameters of this circuit are very small. Therefore, the design of the circuit is reasonable.

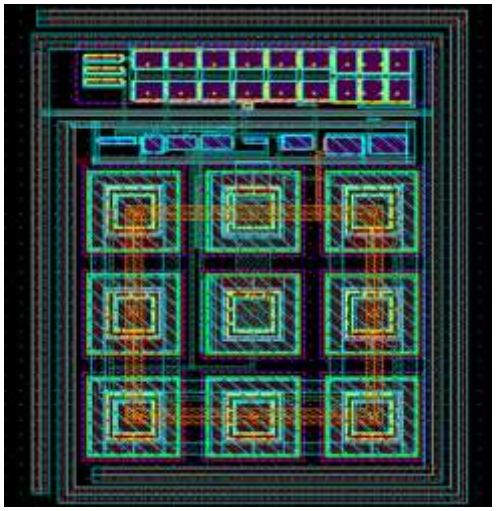

Fig.8Layout of the proposed BGR

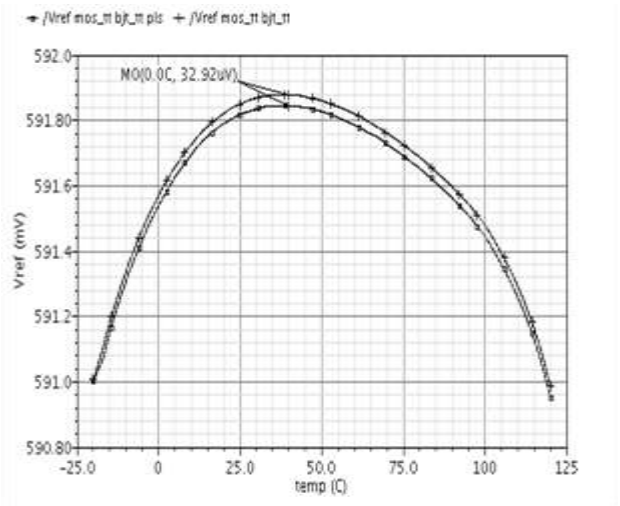

Fig.9Comparison of output voltage Vref versus temperature between simulation and post layout simulation (pls)

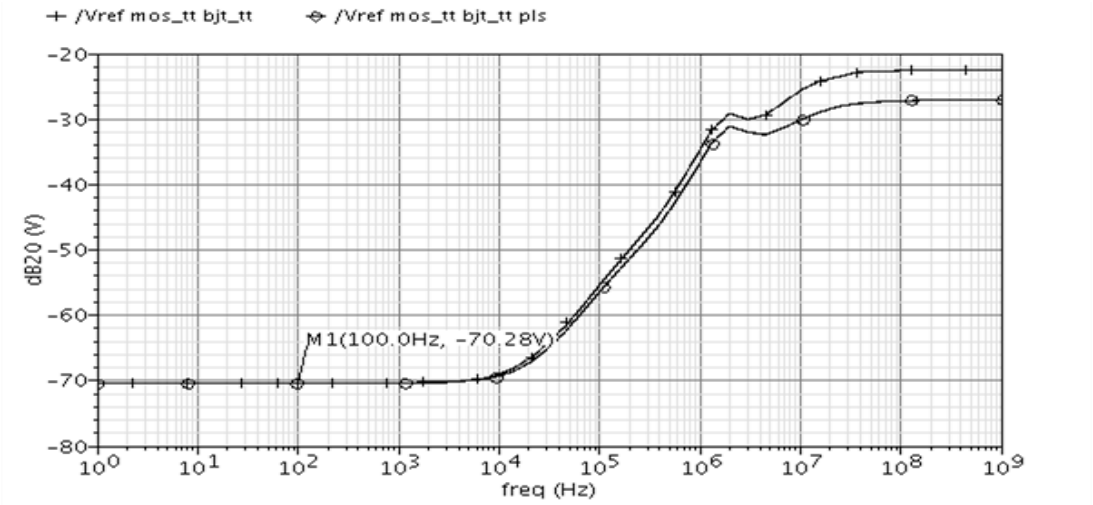

Fig.10Comparison of PSRR versus frequency between simulation and post layout simulation

Table I compares the performance of the voltage references between our circuit and the previous CMOS voltage references [7,9,10]. The voltage reference proposed in this brief shows the better performance in terms of PSRR and TC. Although the circuit in [7] demonstrates a good TC, our design is simpler and needs fewer MOSFETs

Table 1. Comparison With The Reported CMOS Voltage Reference Circuits

	This work	[7]	[9]	[10]
Process	0.18μm	0.35μm	0.5μm	0.13μm
Temperature range	-20-120℃	0-130℃	-55-125℃	-40-85℃
V_{DD}	1.6-3.1V	1.8-4.5 V	1 V	2.5 V
Vref	591.5 mV	847.5 mV	723 mV	1.473 V
TC	10.8 ppm/℃	13.6 ppm/℃	34 ppm/℃	25.3 ppm/℃
Line regulation	0.75 mV/V	0.185 mV/V	1.07 mV/V	NA
PSRR	-70 dB(@100Hz)	-72 dB(@DC)	NA	-27 dB(@DC)
Area	0.012mm^2	0.04 mm^2	0.08 mm^2	0.01 mm^2

V. Conclusion

We have proposed a novel voltage reference consisting of saturated MOSFETs. The circuit generates two voltages with opposite TCs and produces an output voltage with a near-zero TC by adding these TCs together. The design uses the feedback technique instead of operational amplifier to compensate the supply variations. It

is simulated in the 0.18 μm CMOS technology. The results show that TC and line regulation of output voltage are 10.8 ppm/℃ and 0.75 mV/V respectively. PSRR is -70dB, which is greatly improved. The design can monitor the process variation in MOSFET threshold voltage and has its practical value.

VI. Acknowledgements

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